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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,857	01/05/2001	Chien-Meen Hwang	E0869	3692

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EXAMINER	
PATHAK, SUDHANSHU C	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,857	HWANG ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *May 3rd, 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-7 and 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-7 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *January 5th, 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 4-7 & 15-18 are pending in the application.

2. Claims 1-3, 8-14 & 19-22 are cancelled.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 & 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Lin (6,057,789) in further view of Fertner (5742642) in further view of Tice (6,222,456).

Regarding to Claims 4 & 15, the Applicant Admitted Prior Art (AAPA) discloses a network receiver for recovering a frame of data transmitted on a network medium (Specification, Page 1, lines 12-26), the receiver comprising a circuit utilizing a training sequence portion of the data frame for calculating the receiver parameters useful for recovering the transmitted data (Specification, Page 2, lines 5-22). The AAPA further discloses the network receiver wherein the receiver is an equalizer utilizing a complex finite impulse response filter to recover transmitted data and the receiver parameters are coefficients for the filter (Specification, Page 2, lines 5-22). However the AAPA does not disclose the receiver further comprising a buffer circuit storing the data at a first data rate and releasing the data at a second data rate,

slower than the first data rate to effectively reduce the data rate input to the receiver circuit.

Lin discloses a buffer circuit storing the data at a first data rate and releasing the data at a second data rate (Abstract, lines 1-7 & Column 1, lines 14-18, 43-58 & Column 3, lines 25-40 & Column 5, lines 30-56 & Column 7, lines 5-14 & Fig. 2-7). Lin discloses varying the sample rate converter parameters to increase or decrease the data rate of the output data compared to the input data rate (Column 1, lines 43-58 & Column 2, lines 12-38 & Column 5, lines 30-56 & Column 6, lines 10-27 & Column 7, lines 5-52 & Fig. 2-7). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing the sample rate converter as described in Lin in the receiver as described in AAPA reduces the complexity and cost of the digital receiver and can further be integrated on a larger system chip receiver. However, AAPA in view of Lin does not disclose an A/D converter (ADC) to sample the modulated carrier and generate a sequence of samples representing the modulated carrier.

Fertner discloses a digital receiver for use in a network communications system (Fig. 3-4). Fertner further discloses the receiver comprising an analog-to-digital converter (ADC) for sampling a modulated carrier and generating a sequence of sample values representing the modulated carrier (Fig. 4, element 48 & Column 6, lines 15-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the ADC as described in Fertner can be implemented in the digital receiver as

described in AAPA in view of Lin so as to convert the data transmitted into the digital domain to process and recover the transmitted data with minimal errors caused in the transmission medium. However, AAPA in view of Lin in further view of Fertner does not disclose varying the sampling rate depending on the training sequence of the frame or the data portion of the frame.

Tice discloses a detector with a variable sample rate, wherein the detector detects a predetermined profile from the incoming signal using pattern recognition techniques and then varying the sample rate accordingly (Abstract, lines 1-15 & Column 4, lines 8-29). Tice also discloses a programmable processor comprising pattern recognition instructions for detecting the presence of a predetermined profile (Abstract, lines 1-15). Tice also discloses a common control unit, which could be implemented as one, or more interconnected programmed processors and associated, presorted instructions, so as to be implemented in multiple applications (Column 3, lines 25-39). Tice further discloses the detection circuitry and the sampling rate determination circuitry to be coupled to the control circuitry so as to provide processing of the incoming signal (Column 4, lines 39-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Tice teaches that depending on a predetermined sequence of the incoming signal and varying the sampling rate in response to the detected pattern and can be implemented in the receiver as described in AAPA in view of Lin in further view of Fertner and the parameters of the sample rate converter can be varied to a predetermined sampling frequency in response

to the incoming data pattern so as to vary the response time in processing the signal with the predetermined profile. Furthermore, there is no criticality in increasing and decreasing the output sampling frequency of the sample rate converter depending on the type of data is a matter of design choice.

5. Claims 5-6 (apparatus) & 16-17 (method), are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Lin (6,057,789) in further view of Fertner (5,742,642) in further view of Tice (6,222,456) in further view of Liu et al. (6,222,891).

Regarding to Claims 5-6 & 16-17, the Applicant Admitted Prior Art (AAPA) in view of Lin in further view of Fertner in further view of Tice discloses a receiver comprising an A/D converter; and a sample rate converter, to increase or decrease the data rate of the output data compared to the input data rate depending on the data received, further comprising a buffer circuit as described above. However, AAPA in view of Lin in further view of Fertner in further view of Tice does not disclose the receiver comprising a complex mixer receiving the sample values from the A/D converter and generating a sequence of sample values representing an I channel and Q channel data wherein the data transmitted on the network medium utilizing quadrature amplitude modulation (QAM).

Liu discloses a receiver used for receiving digitally modulated signals, using multiple modulation techniques including quadrature amplitude modulation (QAM) (Column 1, lines 50-59, 65-67 & Column 2, lines 3-7 & Column 4, lines 55-65). Liu further discloses the receiver comprising a

complex mixer receiving the sample values from the A/D converter and generating a sequence of sample values representing an I-channel data signal and a sequence of sample values representing a Q-channel data (Fig. 1, element 18 & Column 5, lines 20-33, 46-67 & Column 8, lines 25-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Liu teaches implementing a complex mixer so as to process, receive and demodulate quadrature amplitude modulated transmitted signals, thus satisfying the limitations of the claims.

6. Claims 7 (apparatus) & 18 (method), are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Lin (6,057,789) in further view of Fertner (5,742,642) in further view of Tice (6,222,456) in further view of Liu et al. (6,222,891) in further view of Duan (6,000,834).

Regarding to Claims 7 & 18, the Applicant Admitted Prior Art (AAPA) in view of Lin in further view of Fertner in further view of Tice in further view of Liu discloses a receiver to receive a quadrature amplitude modulated transmitted signal comprising an A/D converter; a complex mixer; and a sample rate converter, to increase or decrease the data rate of the output data compared to the input data rate depending on the data received, further comprising a buffer circuit as described above. However, the references do not disclose a decimation filter to further reduce the sample frequency.

Duan discloses a decimation filter to reduce the sample frequency (Fig. 2, element 32 & Column 1, lines 64-67). Therefore, it would have been obvious

to one of ordinary skill in the art at the time of the invention that Duan teaches implementing a decimation filter to reduce the sample frequency of the incoming samples to provide a more accurate sampled data and this filter can be implemented after the sample rate converter to further reduce the sample frequency, thus satisfying the limitations of the claim.

Response to Arguments

7. Applicant's arguments filed on May 3rd, 2004 have been fully considered but they are not persuasive. Tice teaches implementing a detector circuitry with a variable sample rate, which detects a predetermined profile within the incoming signal, using pattern recognition techniques and then varying the sample rate in response to the detected pattern; the detector along with the control circuitry as described in Tice can be implemented in the receiver as described in AAPA in view of Lin in further view of Fertner so as to vary the sample data rate of the buffer circuit as described in Lin so as to vary the response time in processing the signal with the predetermined profile. The detector and associated circuitry as described in Tice can be implemented to detect the predetermined profile and can be implemented to vary the sample rate converter parameters of the buffer circuit so as to increase or decrease the data rate of the output data compared to the input data rate, thus satisfying the limitations of the claim. Furthermore, there is no criticality in increasing or decreasing the output sampling frequency of the sample rate converter depending on the type of data, it is a matter of design choice and application i.e. increasing or

decreasing the output sampling frequency is dependent on the design and the application the circuitry is implemented in.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (703)-305-0341. The examiner can normally be reached on M-F: 9am-6pm.

   - If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703)-305-4714.
   - The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
   - Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak

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